That Which Is Claimed Is:

1. A method of providing metallurgy structures for input/output pads of an electronic device comprising a substrate including semiconductor portions thereof, and first and second input/output pads on the substrate, the method comprising:

providing first and second metallurgy structures on the respective first and second input/output pads, the first and second metallurgy structures having a shared metallurgy structure adapted to receive solder and wire bonds.

SUB C1

2. A method according to Claim 1 wherein the first and second metallurgy structures comprise a gold layer on a surface thereof opposite the input/output pads.

3. A method according to Claim 1 wherein providing the metallurgy structures comprises:

providing underbump metallurgy layers on the respective input/output pads;

providing barrier layers on the underbump metallurgy layers; and

providing passivation layers on the barrier layers.

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4. A method according to Claim 3 wherein providing underbump metallurgy layers comprises:

providing adhesion layers on the respective input/output pads; and

providing conduction layers on the adhesion layers.

5. A method according to Claim 3 wherein providing underbump metallurgy layers comprises providing a continuous underbump metallurgy layer on the substrate and on the first and second input/output pads.

6. A method according to Claim 5 wherein providing the barrier layers comprises selectively electroplating the barrier layers on the underbump

metallurgy layer and wherein providing the passivation layers comprises selectively electroplating the passivation layers on the barrier layer.

Sub C1 7. A method according to Claim 6 wherein providing the passivation layers is followed by:

removing portions of the continuous underbump metallurgy layer not covered by the barrier layers and the passivation layers.

✓ 8. A method according to Claim 4 wherein the adhesion layers comprise titanium layers, and wherein the conduction layers comprise copper layers.

9. A method according to Claim 3 wherein the barrier layers comprise nickel layers.

10. A method according to Claim 9 wherein the barrier layers have a thickness in a range of 0.5 microns to 2.0 microns.

11. A method according to Claim 3 wherein the passivation layers comprise gold layers.

12. A method according to Claim 11 wherein the gold layers have a thickness in a range of 0.05 microns to 2.0 microns.

13. A method according to Claim 1 further comprising:

providing a solder structure on the first metallurgy structure opposite the substrate; and

maintaining the second metallurgy structure free of solder.

14. A method according to Claim 13 further comprising:

bonding a wire to the second metallurgy structure.

15. A method according to Claim 13 further comprising:

bonding a second substrate to the first substrate via the solder structure.

16. A method according to Claim 1 wherein the electronic device further comprises a protective insulating layer on the substrate and on portions of the first and second input/output pads so that portions of the input/output pads are exposed through the protective insulating layer.

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17. A method for providing a metallurgy structure for an input/output pad of an electronic device comprising a substrate and an input/output pad on the substrate, the method comprising;

providing an underbump metallurgy layer on the input/output pad;

providing a barrier layer on the underbump metallurgy layer; and

providing a passivation layer on the barrier layer.

18. A method according to Claim 17 wherein providing the underbump metallurgy layer comprises:

providing an adhesion layer on the input/output pad; and

providing a conduction layer on the adhesion layer.

19. A method according to Claim 18 wherein providing the adhesion layer comprises providing a titanium layer, and wherein providing the conduction layer comprises providing a copper layer.

20. A method according to Claim 17 wherein the barrier layer comprises a nickel layer.

21. A method according to Claim 20 wherein the barrier layer has a thickness in a range of 0.5 microns to 2.0 microns.

22. A method according to Claim 17 wherein the passivation layer comprises a gold layer.

23. A method according to Claim 22 wherein the gold layer has a thickness in a range of 0.05 microns to 2.0 microns.

24. A method according to Claim 17 further comprising:

providing a solder structure on the metallurgy structure opposite the substrate.

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25. A method according to Claim 24 wherein the electronic device comprises a second input/output pad on the substrate, the method further comprising:

providing a second underbump metallurgy layer on the second input/output pad;

providing a second barrier layer on the second underbump metallurgy layer; and

providing a second passivation layer on the second barrier layer; and

bonding a wire to the second passivation layer.

26. A method according to Claim 24 further comprising:

bonding a second substrate to the first substrate via the solder structure.

27. A method according to Claim 17 further comprising:

a protective insulating layer on the substrate and on portions of the input/output pad so that portions of the input/output pad are exposed through the protective insulating layer.

28. A method according to Claim 17 wherein the passivation layer is adapted to receive solder and wire bonds.

29. An electronic device comprising:

a substrate including semiconductor portions thereof;

first and second input/output pads on the substrate;

first and second metallurgy structures on the respective first and second input/output pads, the first and second metallurgy structures having a shared metallurgy structure adapted to receive solder and wire bonds.

30. An electronic device according to Claim 29 wherein the first and second metallurgy structures each comprise a gold layer on a surface thereof opposite the input/output pads.

31. An electronic device according to Claim 29 wherein the common metallurgy structures each comprise:

an underbump metallurgy layer on the respective input/output pad;

a barrier layer on the underbump metallurgy layer; and

a passivation layer on the barrier layer.

32. An electronic device according to Claim 31 wherein the underbump metallurgy layer comprises an adhesion layer on the respective input/output pad, and a conduction layer on the adhesion layer.

33. An electronic device according to Cliam 32 wherein the adhesion layer comprises a titanium layer, and wherein the conduction layer comprises a copper layer.

34. An electronic device according to Claim 31 wherein the barrier layer comprises a nickel layer.

35. An electronic device according to Claim 34 wherein the barrier layer has a thickness in a range of 0.5 microns to 2.0 microns.

36. An electronic device according to Claim 31 wherein the passivation layer comprises a gold layer.

37. An electronic device according to Claim 36 wherein the gold layer has a thickness in a range of 0.05 microns to 2.0 microns.

38. An electronic device according to Claim 29 further comprising:

a solder structure on the first metallurgy structure opposite the substrate with the second metallurgy structure being free of solder.

39. An electronic device according to Claim 38 further comprising:

a wire bonded to the second metallurgy structure.

40. An electronic device according to Claim 38 further comprising:

a second substrate bonded to the solder structure opposite the first metallurgy structure.

41. An electronic device according to Claim 29 further comprising:

a protective insulating layer on the substrate and on portions of the first and second input/output pads so that portions of the input/output pads are exposed through the protective insulating layer.

42. An electronic device comprising:

a substrate;

an input/output pad on the substrate;

a metallurgy structure on the input/output pad, the metallurgy structure comprising,

an underbump metallurgy layer on the input/output pad;

a barrier layer on the underbump metallurgy layer; and

a passivation layer on the barrier layer.

43. An electronic device according to Claim 42 wherein the under bump metallurgy layer comprises an adhesion layer on the input/output pad, and a conduction layer on the adhesion layer.

44. An electronic device according to Cliam 43 wherein the adhesion layer comprises a titanium layer, and wherein the conduction layer comprises a copper layer.

45. An electronic device according to Claim 42 wherein the barrier layer comprises a nickel layer.

46. An electronic device according to Claim 45 wherein the barrier layer has a thickness in a range of 0.5 microns to 2.0 microns.

47. An electronic device according to Claim 42 wherein the passivation layer comprises a gold layer.

48. An electronic device according to Claim 47 wherein the gold layer has a thickness in a range of 0.05 microns to 2.0 microns.

49. An electronic device according to Claim 42 further comprising:
a solder structure on the metallurgy structure opposite the substrate.

50. An electronic device according to Claim 49 further comprising:
a second input/output pad on the substrate;
a second metallurgy structure on the second input/output pad, the second metallurgy structure comprising,
a second underbump metallurgy layer on the input/output pad,
a second barrier layer on the underbump metallurgy layer, and
a second passivation layer on the barrier layer; and
a wire bonded to the second metallurgy structure.

51. An electronic device according to Claim 49 further compising:
a second substrate bonded to the solder bump opposite the metallurgy structure.

52. An electronic device according to Claim 42 further comprising:
a protective insulating layer on the substrate and on portions of the input/output pad so that portions of the input/output pad are exposed by the protective insulating layer.

53. An electronic device according to Claim 42 wherein the passivation layer is adapted to receive solder and wire bonds.

54. An electronic device comprising:

a substrate;

an input/output pad on the substrate;

a bonding structure on the input/output pad, the bonding structure comprising,

a barrier layer comprising nickel on the input/output pad; and

a solder structure on the barrier layer.

55. An electronic device according to Claim 54 further comprising an under bump metallurgy layer between the nickel barrier layer and the input/output pad.

56. A electronic device according to Claim 55 wherein the under bump metallurgy layer comprises an adhesion layer on the input/output pad, and a conduction layer on the adhesion layer.

57. An electronic device according to Claim 56 wherein the adhesion layer comprises a titanium layer, and wherein the conduction layer comprises a copper layer.

58. An electronic device according to Claim 54 wherein the barrier layer comprises a nickel layer free of lead and an alloy layer including nickel and lead between the nickel layer free of lead and the solder structure.

59. An electronic device according to Claim 54 further comprising:

a second input/output pad on the substrate;

a second bonding structure on the second input/output pad, the second bonding structure comprising,

a second barrier layer comprising nickel on the second input/output pad, and

a gold layer on the barrier layer comprising nickel; and

a wire bonded to the second bonding structure.

60. An electronic device according to Claim 54 further compising:

a second substrate bonded to the solder structure.

61. An electronic device according to Claim 54 further comprising:

a protective insulating layer on the substrate and on portions of the input/output pad so that portions of the input/output pad are exposed through the protective insulating layer.

62. A method for providing bonding structures for input/output pads of an electronic device comprising a substrate and first and second input/output pads on the substrate, the method comprising;

providing first and second barrier layers on the respective first and second input/output pads wherein the first and second barrier layers each comprise nickel;

providing first and second passivation layers on the respective first and second barrier layers; and

providing a solder structure on the first passivation layer while maintaining the second passivation layer free of solder.

63. A method according to Claim 62 further comprising:

providing first and second under bump metallurgy layers between the first and second barrier layers and the first and second input/output pads.

64. A method according to Claim 62 further comprising:

reflowing the solder structure so that the first passivation layer diffuses into the solder structure.

65. A method according to Claim 64 wherein during reflowing the solder structure, lead from the solder structure diffuses into a portion of the first barrier layer.

66. A method according to Claim 62 further comprising:

bonding a wire to the second passivation layer.

67. A method according to Claim 62 wherein the passivation layer comprises a gold layer.

68. A method according to Claim 62 further comprising:

bonding a second substrate to the first substrate via the solder structure.